

General Description

The MY80N08NE5 uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.

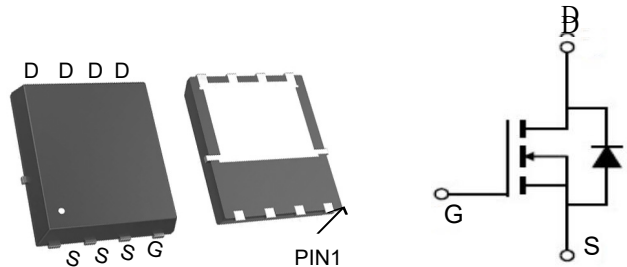


Features

V_{DSS}	80	V
I_D	80	A
$R_{DS(ON)}(at V_{GS}=10V)$	<4.8	m Ω
$R_{DS(ON)}(at V_{GS}=4.5V)$	<6.3	m Ω

Application

- Battery protection
- Load switch
- Uninterruptible power supply



Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
MY80N08NE5	PDFN5*6-8L	NULL	5000

Absolute Maximum Ratings ($T_C=25^{\circ}\text{C}$ unless otherwise noted)

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	80	V
V_{GS}	Gate-Source Voltage	± 20	V
$I_D@T_C=25^{\circ}\text{C}$	Continuous Drain Current, $V_{GS} @ 10V^{1,6}$	80	A
$I_D@T_C=100^{\circ}\text{C}$	Continuous Drain Current, $V_{GS} @ 10V^{1,6}$	42.5	A
I_{DM}	Pulsed Drain Current ²	170	A
E_{AS}	Single Pulse Avalanche Energy ³	57.8	mJ
I_{AS}	Avalanche Current	34	A
$P_D@T_C=25^{\circ}\text{C}$	Total Power Dissipation ⁴	56	W
T_{STG}	Storage Temperature Range	-55 to 150	$^{\circ}\text{C}$
T_J	Operating Junction Temperature Range	-55 to 150	$^{\circ}\text{C}$
$R_{\theta JA}$	Thermal Resistance Junction-Ambient ¹	62	$^{\circ}\text{C/W}$
$R_{\theta JC}$	Thermal Resistance Junction-Case ¹	2.2	$^{\circ}\text{C/W}$

Electrical Characteristics ($T_J=25\text{ }^{\circ}\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V$, $I_D=250\mu A$	80	---	---	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance ²	$V_{GS}=10V$, $I_D=20A$	---	4.8	6.5	m Ω
$R_{DS(ON)}$	Static Drain-Source On-Resistance ²	$V_{GS}=4.5V$, $I_D=20A$	---	6.3	8.5	m Ω
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS}=V_{DS}$, $I_D=250\mu A$	1.0	---	2.5	V
I_{DSS}	Drain-Source Leakage Current	$V_{DS}=64V$, $V_{GS}=0V$, $T_J=25\text{ }^{\circ}\text{C}$	---	---	1	μA
		$V_{DS}=64V$, $V_{GS}=0V$, $T_J=55\text{ }^{\circ}\text{C}$	---	---	5	
I_{GSS}	Gate-Source Leakage Current	$V_{GS}=\pm 20V$, $V_{DS}=0V$	---	---	± 100	nA
g_{fs}	Forward Transconductance	$V_{DS}=5V$, $I_D=20A$	---	75	---	S
R_g	Gate Resistance	$V_{DS}=0V$, $V_{GS}=0V$, $f=1\text{MHz}$	---	0.5	---	Ω
Q_g	Total Gate Charge (10V)	$V_{DS}=40V$, $V_{GS}=10V$, $I_D=20A$	---	40	---	nC
Q_{gs}	Gate-Source Charge		---	7.2	---	
Q_{gd}	Gate-Drain Charge		---	6.5	---	
$T_{d(on)}$	Turn-On Delay Time	$V_{DD}=40V$, $V_{GS}=10V$, $R_G=3\Omega$, $I_D=20A$	---	8.3	---	ns
T_r	Rise Time		---	4.2	---	
$T_{d(off)}$	Turn-Off Delay Time		---	36	---	
T_f	Fall Time		---	6.9	---	
C_{iss}	Input Capacitance	$V_{DS}=40V$, $V_{GS}=0V$, $f=1\text{MHz}$	---	2860	---	pF
C_{oss}	Output Capacitance		---	410	---	
C_{rss}	Reverse Transfer Capacitance		---	38	---	
I_S	Continuous Source Current ^{1,5}	$V_G=V_D=0V$, Force Current	---	---	48	A
V_{SD}	Diode Forward Voltage ²	$V_{GS}=0V$, $I_S=A$, $T_J=25\text{ }^{\circ}\text{C}$	---	0.77	1.0	V
t_{rr}	Reverse Recovery Time	$I_F=20A$, $di/dt=100A/\mu s$, $T_J=25\text{ }^{\circ}\text{C}$	---	27	---	nS
Q_{rr}	Reverse Recovery Charge		---	89	---	nC

Note :

- 1.The data tested by surface mounted on a 1 inch² FR-4 board with 20Z copper.
- 2.The data tested by pulsed , pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$
- 3.The EAS data shows Max. rating . The test condition is $V_{DD}=25V$, $V_{GS}=10V$, $L=0.1mH$, $I_{AS}=34A$
- 4.The power dissipation is limited by 150 $^{\circ}\text{C}$ junction temperature
- 5.The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.
- 6.The maximum current rating is package limited.

Typical Characteristics

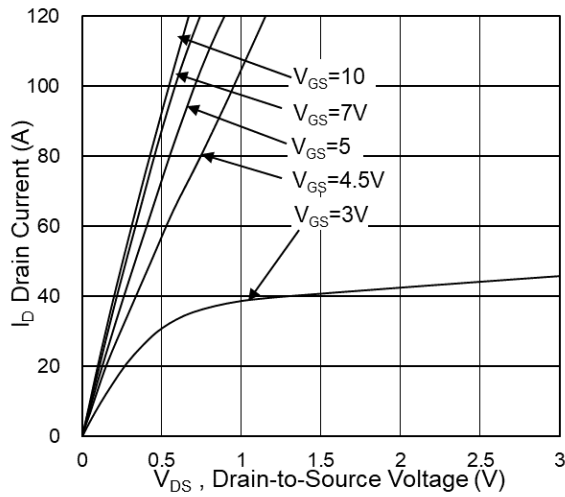


Fig.1 Typical Output Characteristics

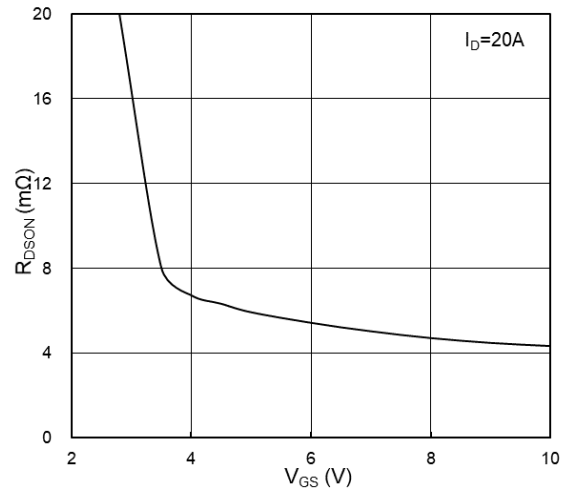


Fig.2 On-Resistance vs G-S Voltage

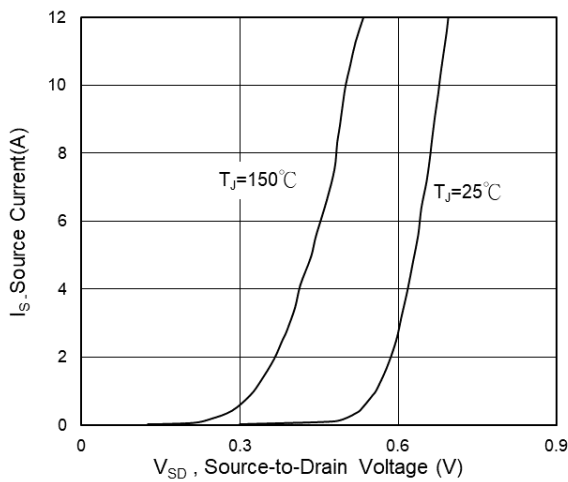


Fig.3 Source Drain Forward Characteristics

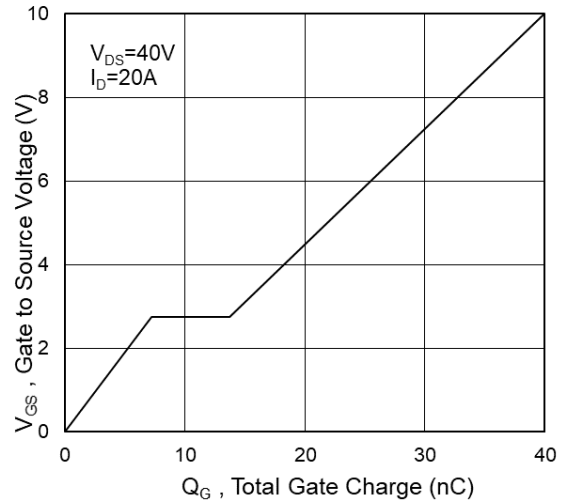


Fig.4 Gate-Charge Characteristics

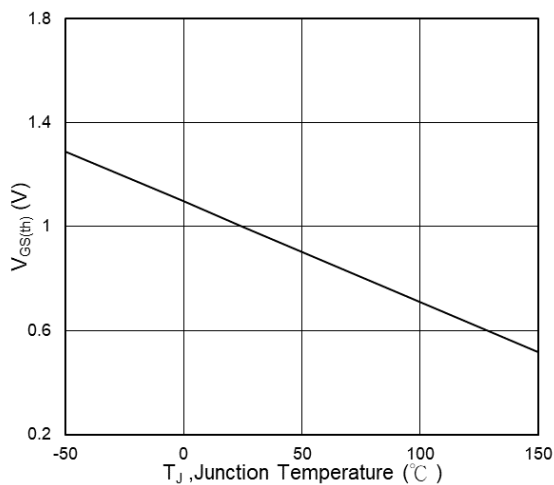


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

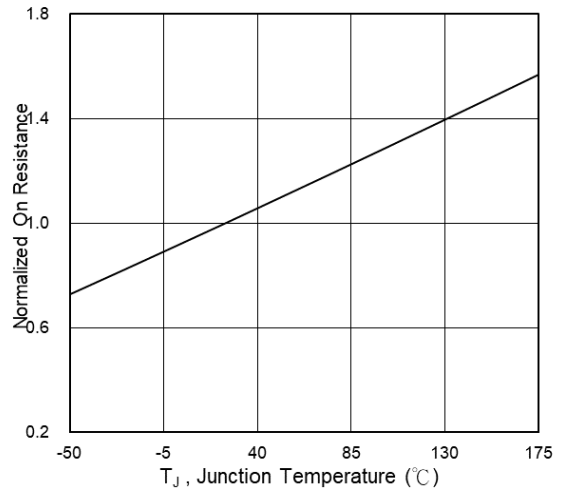


Fig.6 Normalized $R_{DS(on)}$ vs. T_J

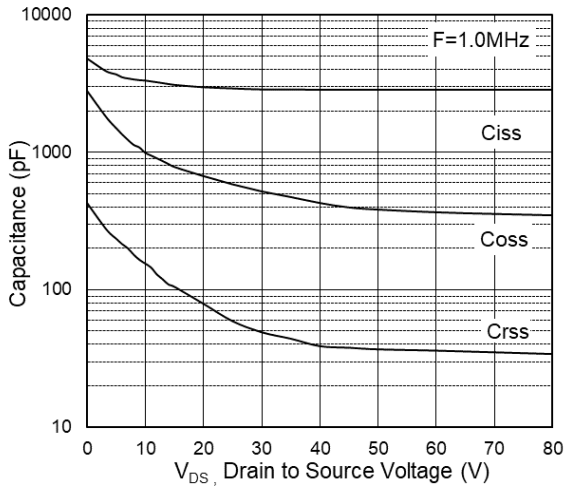


Fig.7 Capacitance

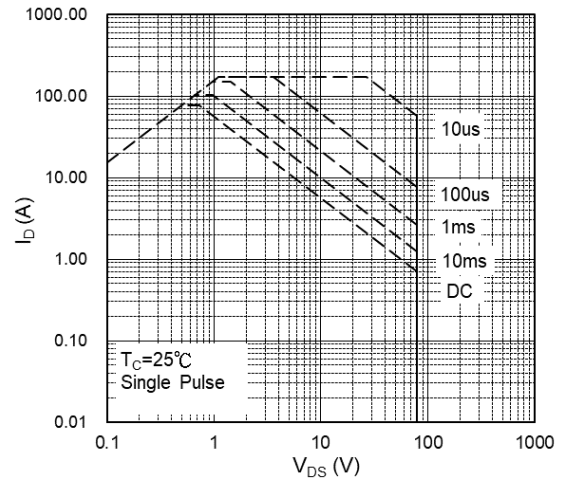


Fig.8 Safe Operating Area

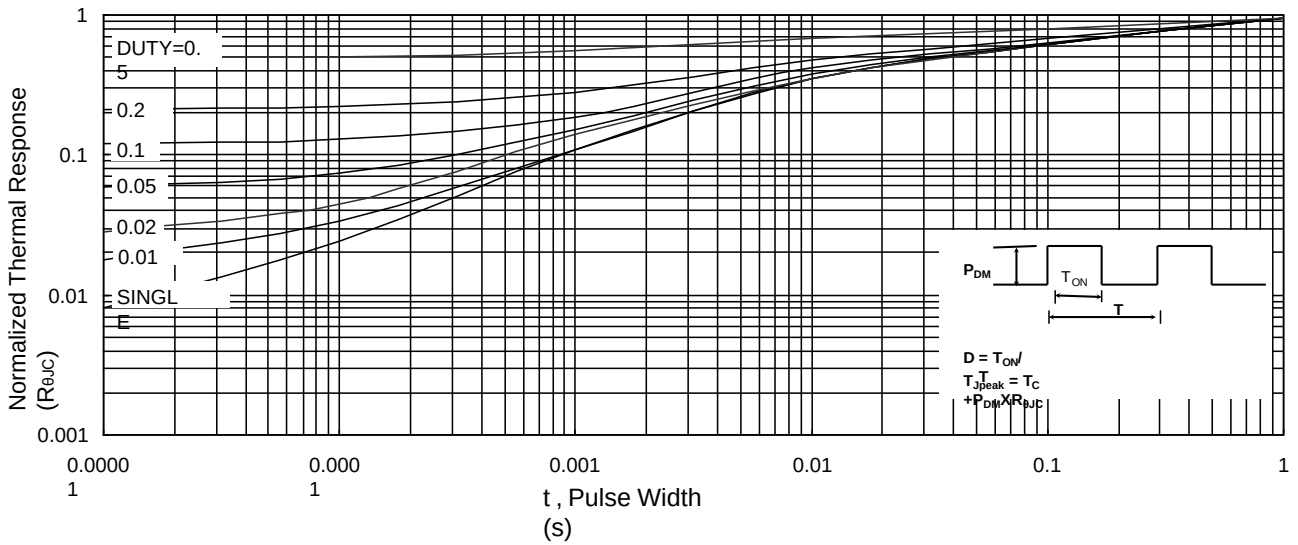


Fig.9 Normalized Maximum Transient Thermal Impedance

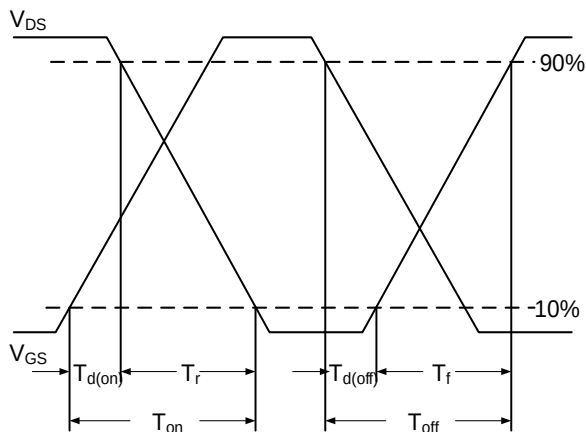


Fig.10 Switching Time Waveform

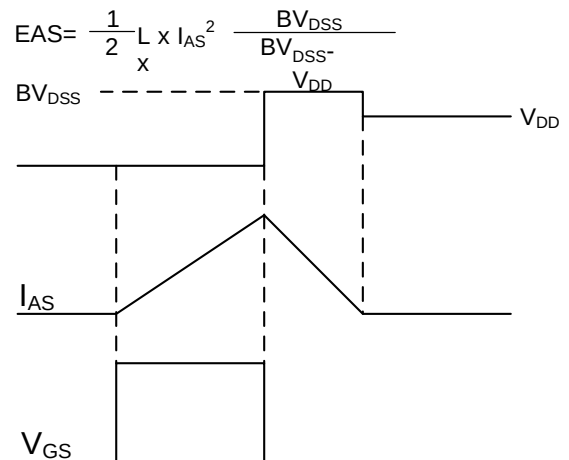
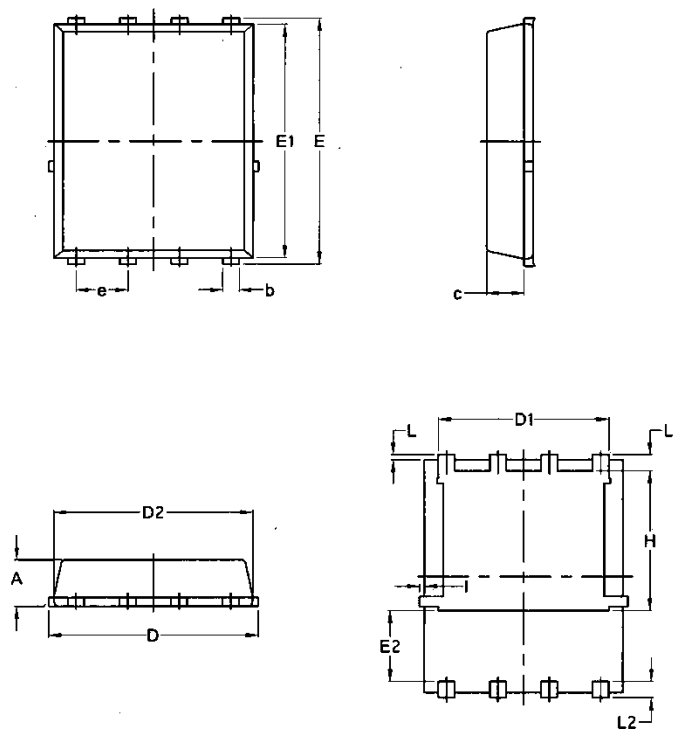


Fig.11 Unclamped Inductive Switching Waveform

Package Mechanical Data-DFN5*6-8L-JQ Single



Symbol	Common			
	mm		Inch	
	Mim	Max	Min	Max
A	1.03	1.17	0.0406	0.0461
b	0.34	0.48	0.0134	0.0189
c	0.824	0.0970	0.0324	0.082
D	4.80	5.40	0.1890	0.2126
D1	4.11	4.31	0.1618	0.1697
D2	4.80	5.00	0.1890	0.1969
E	5.95	6.15	0.2343	0.2421
E1	5.65	5.85	0.2224	0.2303
E2	1.60	/	0.0630	/
e	1.27 BSC		0.05 BSC	
L	0.05	0.25	0.0020	0.0098
L1	0.38	0.50	0.0150	0.0197
L2	0.38	0.50	0.0150	0.0197
H	3.30	3.50	0.1299	0.1378
I	/	0.18	/	0.0070