

General Description

The MY10N40T N-channel enhanced vdmofets, is obtained by the self-aligned planar technology which reduce the conduction loss, improve switching performance and enhance the avalanche energy. Which accords with the RoHS standard

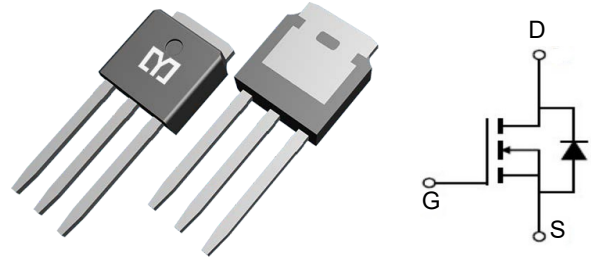


Features

V_{DSS}	400	V
I_D	10	A
P_D ($T_C=25^{\circ}C$)	100	W
$R_{DS(ON)}$ (at $V_{GS}=10V$)	<0.55	Ω

Application

- Fast switching
- Low on-resistance
- ULow gate charge and input capacitance
100% avalanche tested



Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
MY10N40T	TO-251	10N40	2500

Absolute Maximum Ratings ($T_C=25^{\circ}C$ unless otherwise noted)

Parameter	Symbol	MY10N40T	Unit
Drain-Source Voltage	V_{DS}	400	V
Gate-Source Voltage	V_{GS}	± 30	V
Continuous Drain Current	I_D	$T_C=25^{\circ}C$ 10	A
		$T_C=100^{\circ}C$ 6.3	
Pulsed Drain Current (Note 1)	I_{DM}	40	A
Single Pulse Avalanche Energy(Note 2)	E_{AS}	450	mJ
Avalanche Current(Note 1)	I_{AR}	-	A
Power Dissipation $T_C=25^{\circ}C$	P_D	100	W
Operating Junction and Storage Temperature	T_J/T_{STG}	-55~+175	$^{\circ}C$

Gate-Source Voltage

Parameter	Symbol	MY10N40T	Unit
Thermal resistance Junction to Ambient	$R_{\theta JA}$	62.5	$^{\circ}\text{C/W}$
Thermal resistance Junction to Case	$R_{\theta JC}$	1.25	$^{\circ}\text{C/W}$

Electrical Characteristics ($T_J=25^{\circ}\text{C}$, unless otherwise noted)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Off Characteristics							
Drain-Source Breakdown Voltage		BV _{DSS}	V _{GS} =0V,I _D =250μA	400	-	-	V
Drain-Source Leakage Current		I _{DSS}	V _{DS} =400V,V _{GS} =0V	-	-	1	μA
Gate- Source Leakage Current	Forward	I _{GSS}	V _{GS} =30V,V _{DS} =0V	-	-	100	nA
	Reverse		V _{GS} =-30V,V _{DS} =0V	-	-	-100	nA
On Characteristics(Note 4)							
Gate Threshold Voltage		V _{GS(TH)}	V _{DS} =V _{GS} ,I _D =250μA	2.0	3.0	4.0	V
Static Drain-Source On-State Resistance		R _{DS(ON)}	V _{GS} =10V,I _D =5A	-	0.44	0.55	Ω
Dynamic Characteristics(Note 5)							
Input Capacitance		C _{ISS}	V _{DS} =25V,V _{GS} =0V,f=1MHz	-	1126	-	pF
Output Capacitance		C _{OSS}		-	124	-	pF
Reverse Transfer Capacitance		C _{RSS}		-	8	-	pF
Switching Characteristics (Note 5)							
Turn-On Delay Time		td(on)	V _{DD} =200V,I _D =10A, R _G =10Ω	-	18	-	ns
Turn-On Rise Time		t _R		-	23	-	ns
Turn-Off Delay Time		td(off)		-	41	-	ns
Turn-Off Fall Time		t _f		-	19	-	ns
Total Gate Charge		Q _G	V _{DD} =320V,I _D =10A, V _{GS} =10V	-	23	-	nC
Gate-Source Charge		Q _{GS}		-	5.2	-	nC
Gate-Drain Charge		Q _{GD}		-	8.5	-	nC
Drain-Source Diode Characteristics and Maximum Ratings							
Drain-Source Diode Forward Voltage		V _{SD}	V _{GS} =0V, I _S =10A	-	-	1.5	V
Maximum Continuous Drain-Source Diode Forward Current		I _S		-	-	10	A
Reverse Recovery Time		trr	V _{GS} =0V, I _F =10A	-	376	-	ns
Reverse Recovery Charge		Q _{RR}	dl _F /dt=100A/μs (Note 1)	-	2560	-	nC

Notes : 1 Repetitive Rating:Pulse width limited by maximum junction temperature

2 $L=10\text{mH}, I_D=9.5A, V_{DD}=50V$, Starting $T_J=25^{\circ}\text{C}$

4 Pulse Test: Pulse width $\leq 300\mu s$, Duty cycle $\leq 2\%$

5 Guaranteed by design, not subject to production

Typical Characteristics

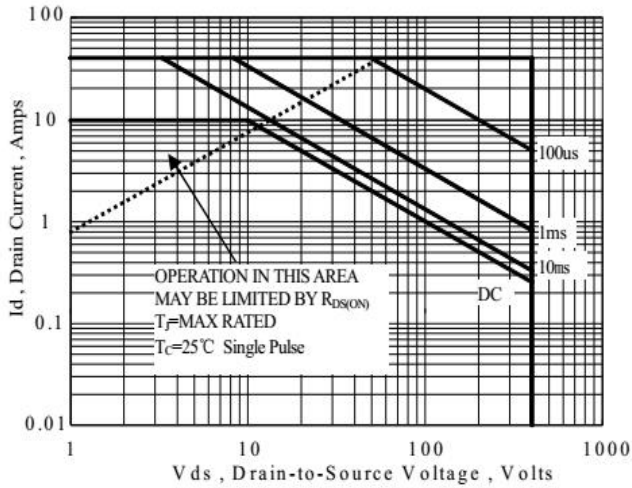


Figure 1 Maximum Forward Bias Safe Operating Area

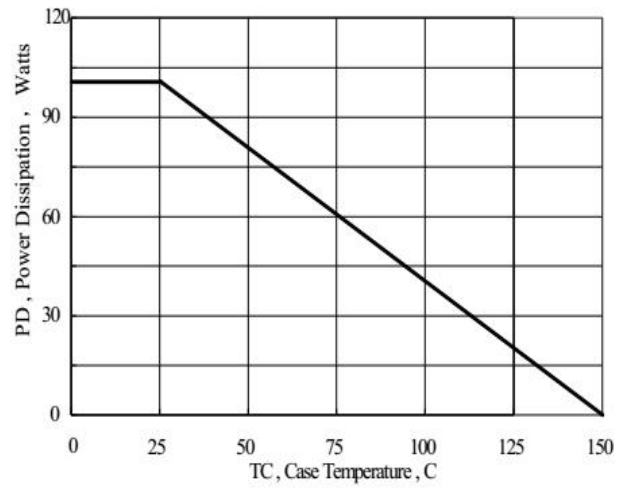


Figure 2 Maximum Power Dissipation vs Case Temperature

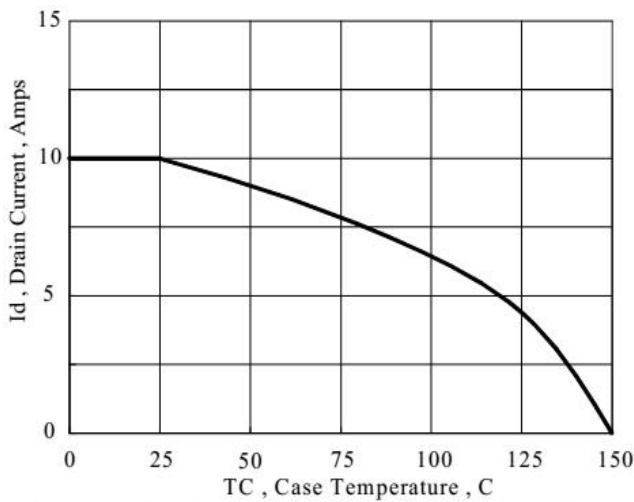


Figure 3 Maximum Continuous Drain Current vs Case Temperature

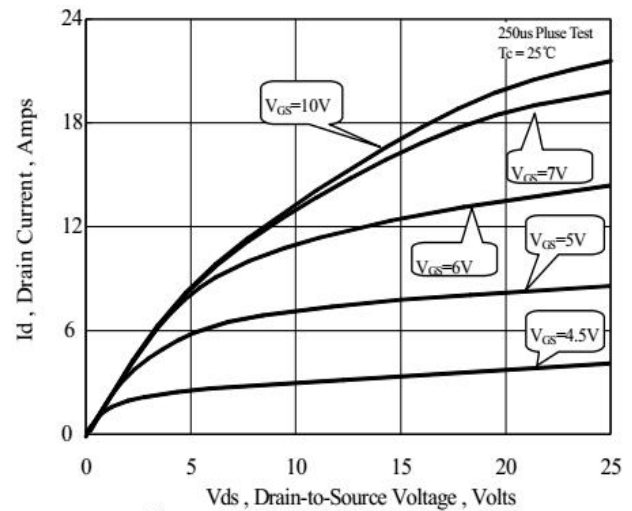


Figure 4 Typical Output Characteristics

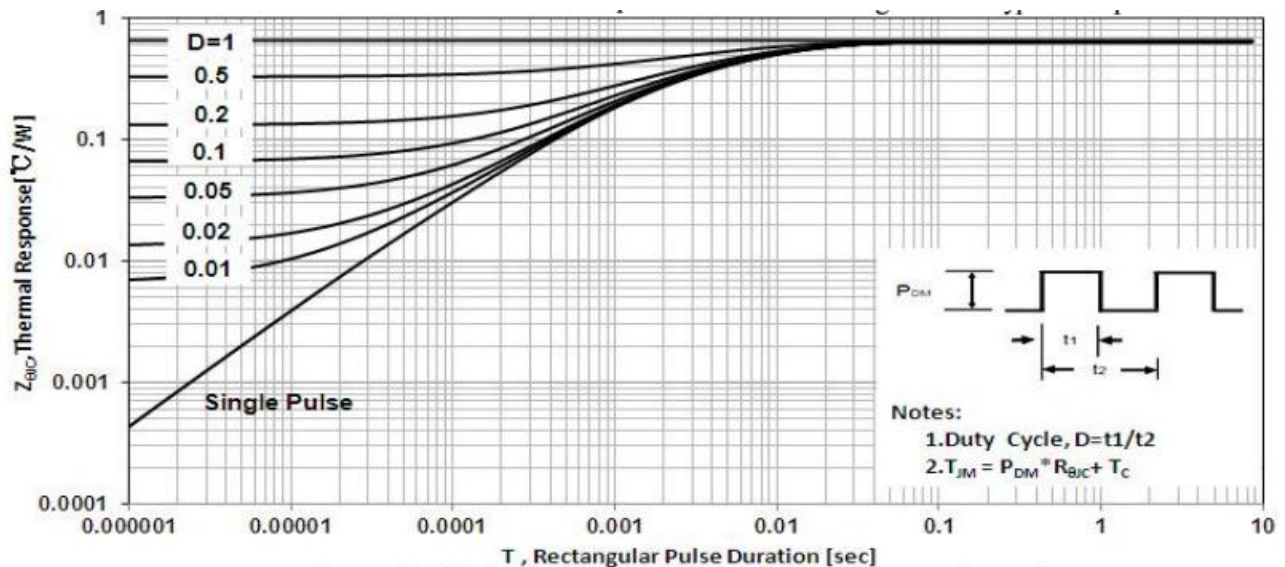


Figure 5 Maximum Effective Thermal Impedance, Junction to Case

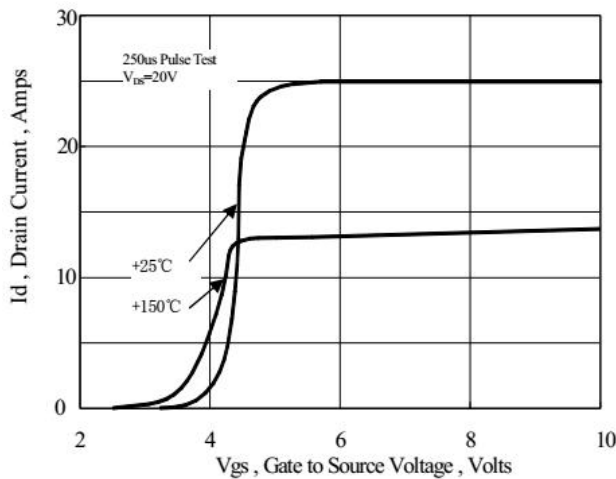


Figure 6 Typical Transfer Characteristics

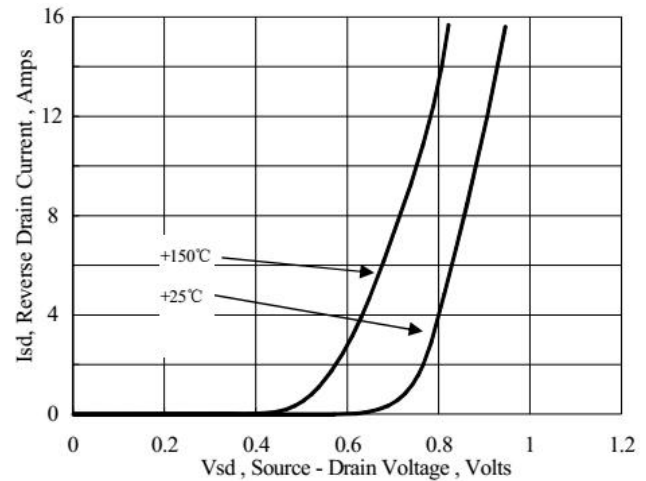


Figure 7 Typical Body Diode Transfer Characteristics

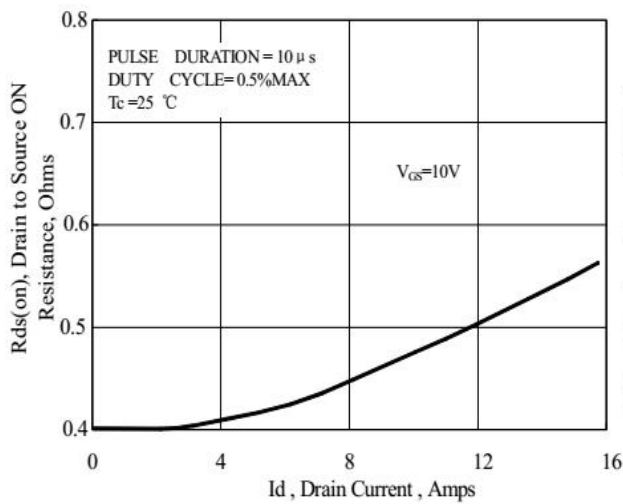


Figure 8 Typical Drain to Source ON Resistance vs Drain Current

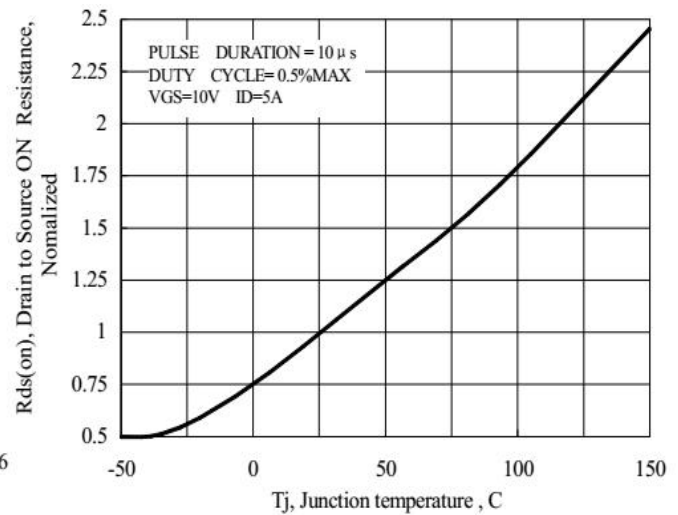


Figure 9 Typical Drain to Source on Resistance vs Junction Temperature

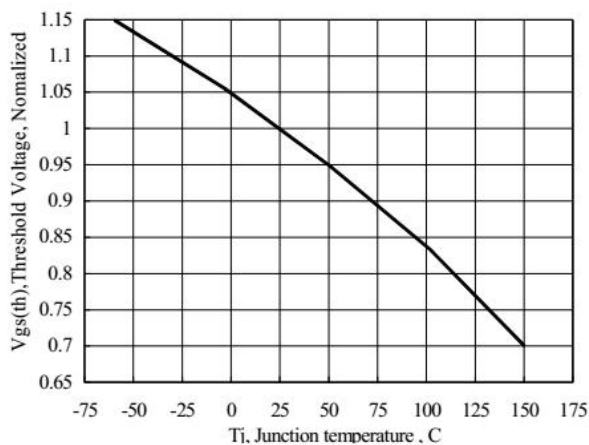


Figure 10 Typical Threshold Voltage vs Junction Temperature

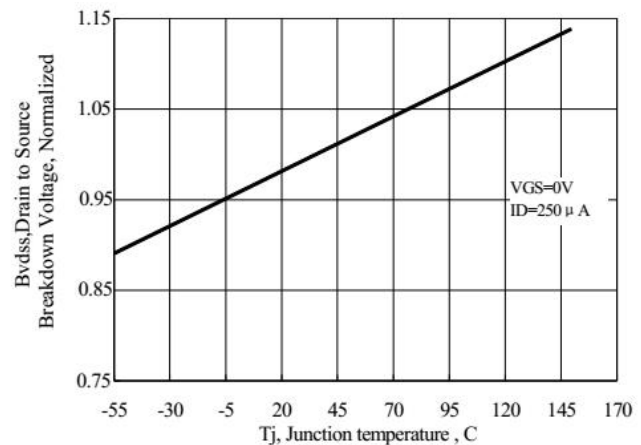


Figure 11 Typical Breakdown Voltage vs Junction Temperature

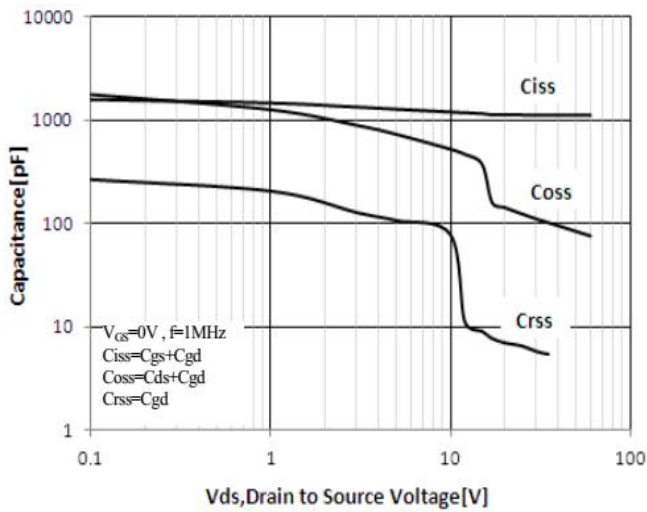


Figure 12 Typical Capacitance vs Drain to Source Voltage

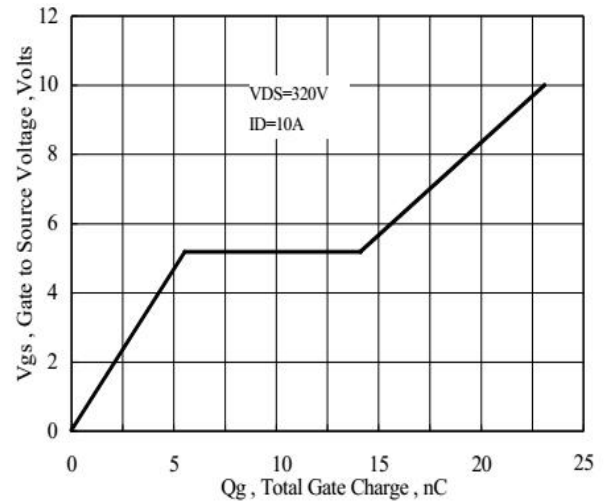


Figure 13 Typical Gate Charge vs Gate to Source Voltage

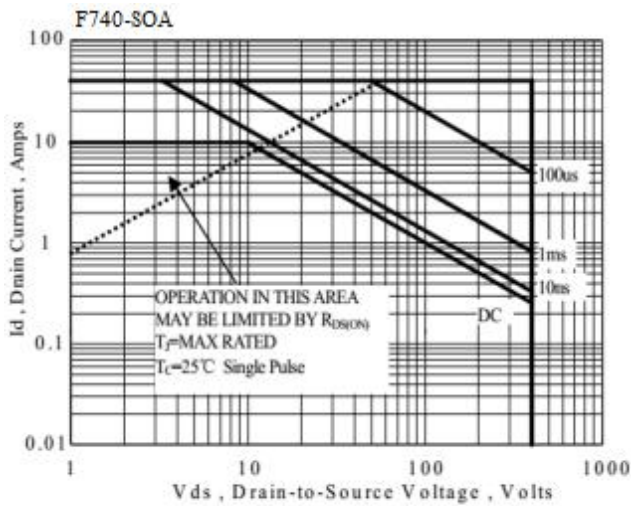


Figure 14 Maximum Forward Bias Safe Operating Area

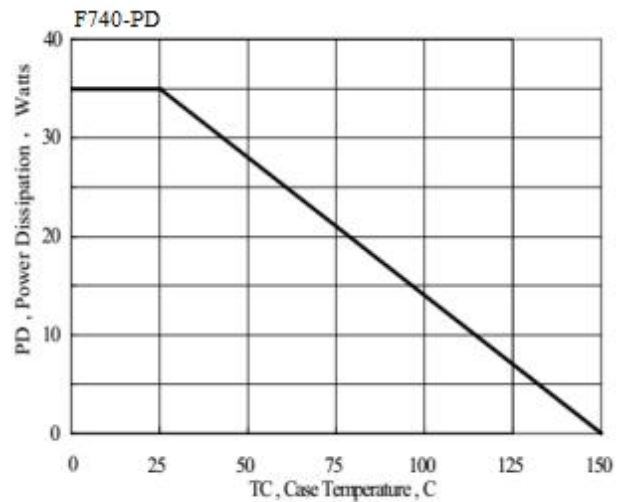


Figure 15 Maximum Power Dissipation vs Case Temperature

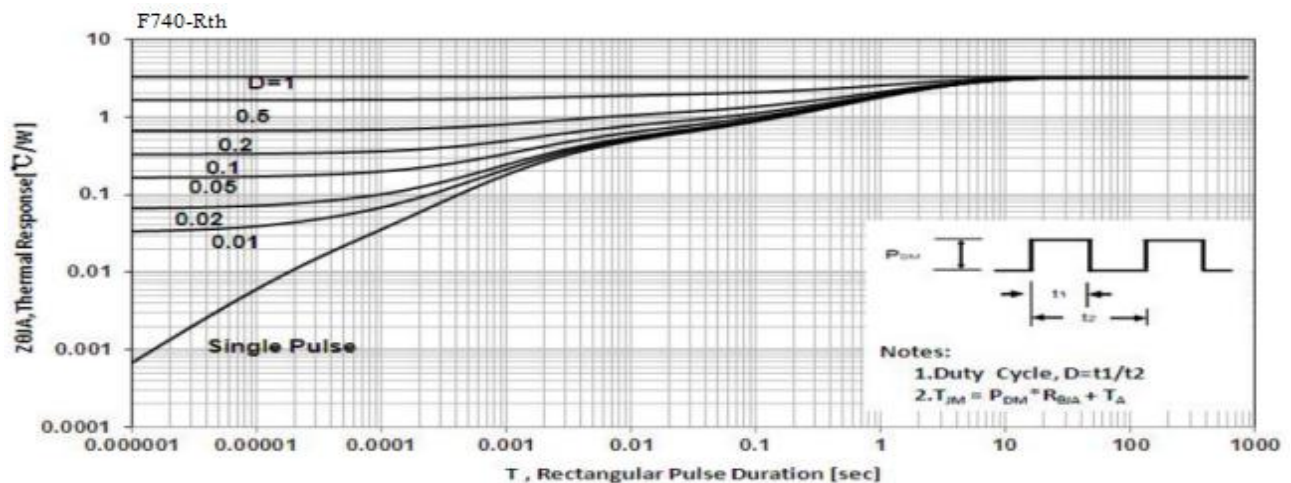
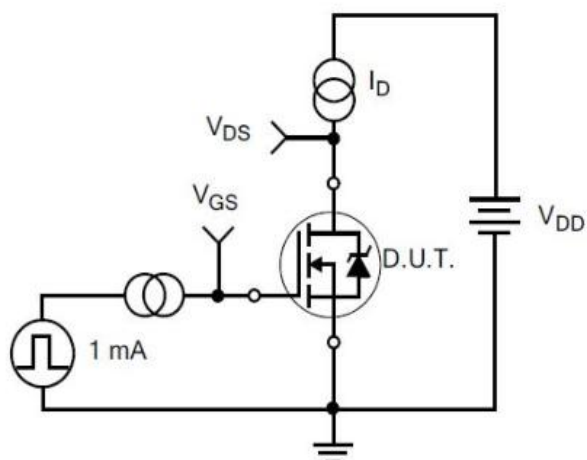
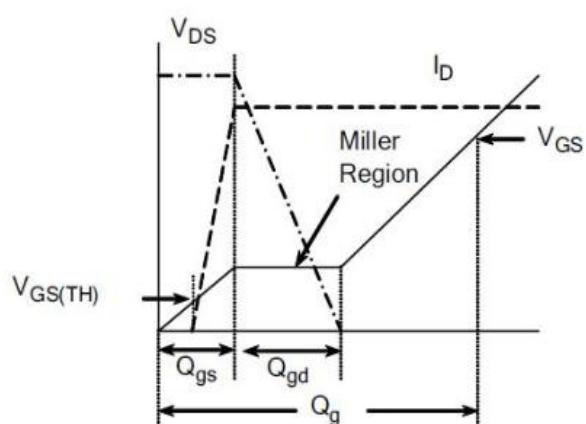


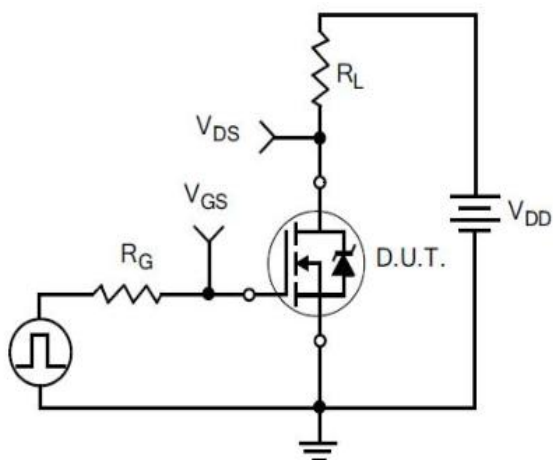
Figure 16 Maximum Effective Thermal Impedance, Junction to Case



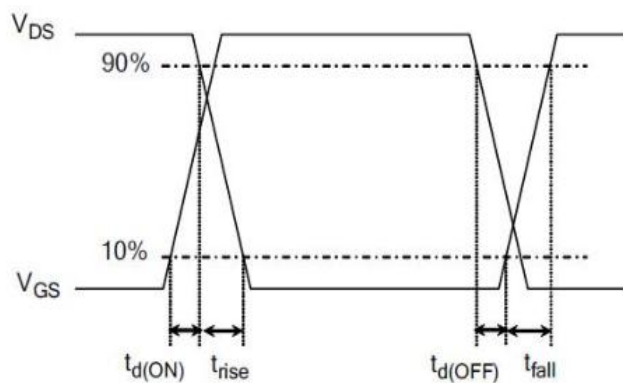
1) Gate Charge Test Circuit



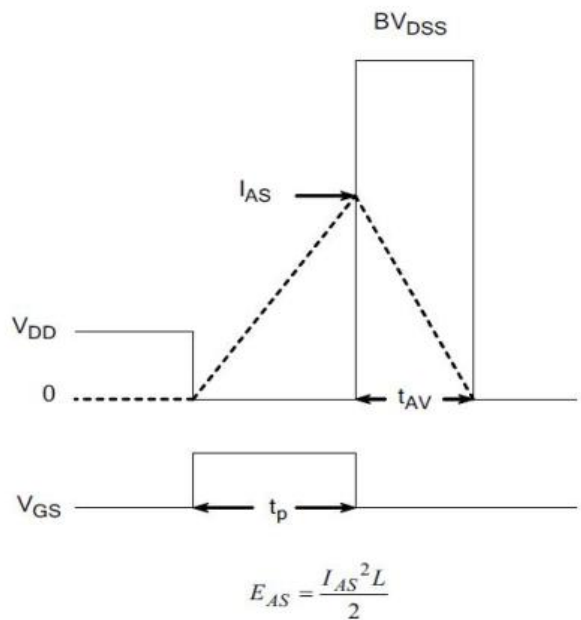
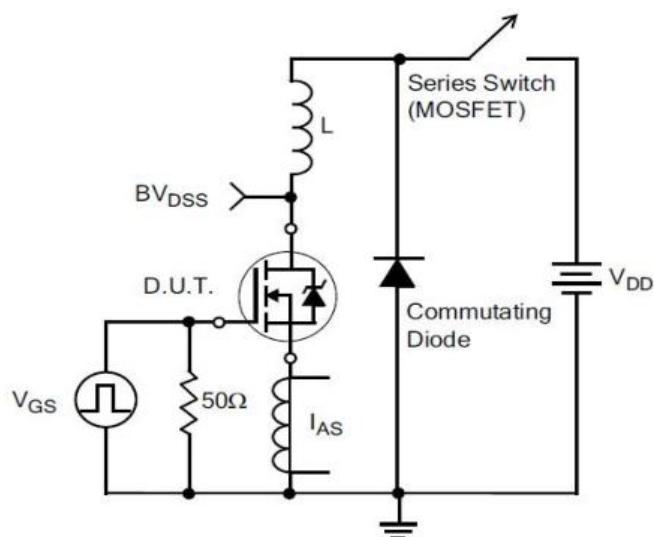
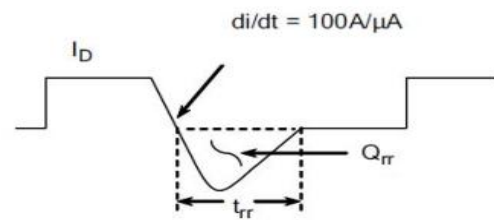
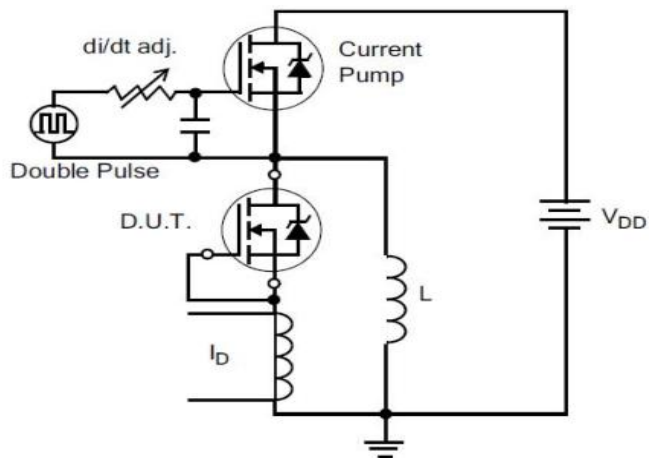
2) . Gate Charge Waveform



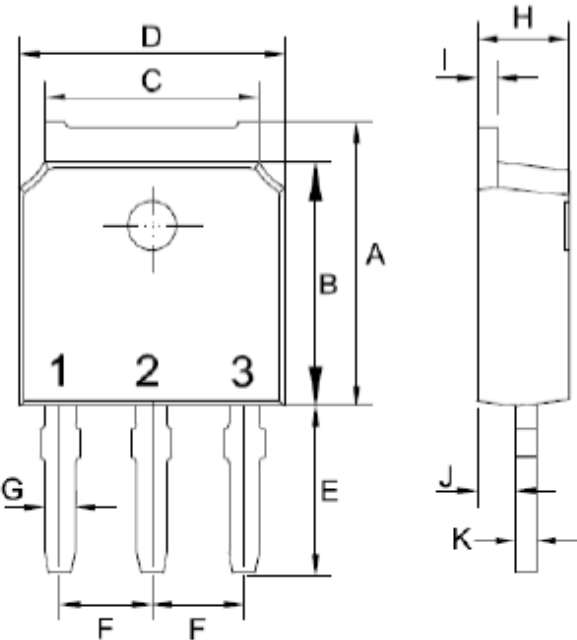
3) Resistive Switching Test Circuit



4) Resistive Switching Waveforms



Package Mechanical Data-TO-251-JQ Single



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	6.85	7.25	0.270	0.285
B	5.8	6.3	0.228	0.248
C	5	5.53	0.197	0.218
D	6.3	6.8	0.248	0.268
E	3.5	4.35	0.138	0.171
F	2.19	2.39	0.086	0.094
G	0.45	0.85	0.018	0.033
H	2.2	2.4	0.087	0.094
I	0.41	0.61	0.016	0.024
J	0.71	1.31	0.028	0.052
K	0.41	0.61	0.016	0.024