

General Description

The MY018FNC uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.

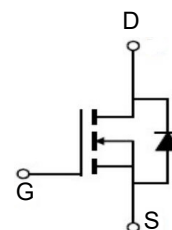
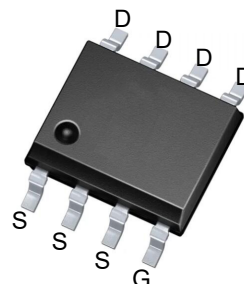


Features

V_{DSS}	60	V
I_D	15	A
$P_D(T_A=25^{\circ}C)$	1.5	W
$R_{DS(ON)}(at V_{GS}=10V)$	<18	m Ω

Application

- Battery protection
- Load switch
- Uninterruptible power supply



Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
MY018FNC	SOP-8	018FNC	3000

Absolute Maximum Ratings ($T_C=25^{\circ}C$ unless otherwise noted)

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	60	V
V_{GS}	Gate-Source Voltage	± 20	V
$I_D@T_A=25^{\circ}C$	Continuous Drain Current, V_{GS} @ 10V ¹	15	A
$I_D@T_A=70^{\circ}C$	Continuous Drain Current, V_{GS} @ 10V ¹	5	A
I_{DM}	Pulsed Drain Current ²	32	A
EAS	Single Pulse Avalanche Energy ³	18	mJ
I_{AS}	Avalanche Current	28	A
$P_D@T_A=25^{\circ}C$	Total Power Dissipation ⁴	1.5	W
T_{STG}	Storage Temperature Range	-55 to 150	$^{\circ}C$
T_J	Operating Junction Temperature Range	-55 to 150	$^{\circ}C$
$R_{\theta JA}$	Thermal Resistance Junction-Ambient ¹	85	$^{\circ}C/W$
$R_{\theta JC}$	Thermal Resistance Junction-Case ¹	25	$^{\circ}C/W$

Electrical Characteristics ($T_J=25^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V$, $I_D=250\mu A$	60	---	---	V
$\Delta BV_{DSS}/\Delta T_J$	BV_{DSS} Temperature Coefficient	Reference to 25°C , $I_D=1mA$	---	0.057	---	$V/^\circ\text{C}$
$R_{DS(ON)}$	Static Drain-Source On-Resistance ²	$V_{GS}=10V$, $I_D=6A$	---	15	18	$m\Omega$
		$V_{GS}=4.5V$, $I_D=4A$	---	18	20	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS}=V_{DS}$, $I_D=250\mu A$	1.2	---	2.5	V
$\Delta V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient		---	-5.68	---	$mV/^\circ\text{C}$
I_{DSS}	Drain-Source Leakage Current	$V_{DS}=48V$, $V_{GS}=0V$, $T_J=25^\circ\text{C}$	---	---	1	μA
		$V_{DS}=48V$, $V_{GS}=0V$, $T_J=55^\circ\text{C}$	---	---	5	
I_{GSS}	Gate-Source Leakage Current	$V_{GS}=\pm 20V$, $V_{DS}=0V$	---	---	± 100	nA
g_{fs}	Forward Transconductance	$V_{DS}=5V$, $I_D=6A$	---	40	---	S
R_g	Gate Resistance	$V_{DS}=0V$, $V_{GS}=0V$, $f=1MHz$	---	1.7	---	Ω
Q_g	Total Gate Charge (4.5V)	$V_{DS}=48V$, $V_{GS}=4.5V$, $I_D=6A$	---	18.8	---	nC
Q_{gs}	Gate-Source Charge		---	7.7	---	
Q_{gd}	Gate-Drain Charge		---	6.2	---	
$T_{d(on)}$	Turn-On Delay Time	$V_{DD}=30V$, $V_{GS}=10V$, $R_G=3.3\Omega$, $I_D=6A$	---	7.6	---	ns
T_r	Rise Time		---	8.6	---	
$T_{d(off)}$	Turn-Off Delay Time		---	47	---	
T_f	Fall Time		---	4	---	
C_{iss}	Input Capacitance	$V_{DS}=15V$, $V_{GS}=0V$, $f=1MHz$	---	960	---	pF
C_{oss}	Output Capacitance		---	113	---	
C_{rss}	Reverse Transfer Capacitance		---	97	---	
I_S	Continuous Source Current ^{1,5}	$V_G=V_D=0V$, Force Current	---	---	6.3	A
I_{SM}	Pulsed Source Current ^{2,5}		---	---	32	A
V_{SD}	Diode Forward Voltage ²	$V_{GS}=0V$, $I_S=A$, $T_J=25^\circ\text{C}$	---	---	1	V
t_{rr}	Reverse Recovery Time	$I_F=6A$, $dI/dt=100A/\mu s$, $T_J=25^\circ\text{C}$	---	15	---	nS
Q_{rr}	Reverse Recovery Charge		---	10.4	---	nC

Note :

1.The data tested by surface mounted on a 1 inch² FR-4 board with 20Z copper. 2 .The data tested by pulsed , pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$

3 .The EAS data shows Max. rating . The test condition is V.The power dissipation is limited by 150^oC junction temperature $V_{DS}=25V$, $V_{GS}=10V$, $L=0.1mH$, $I_{AS}=28A$

4 .The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

Typical Characteristics

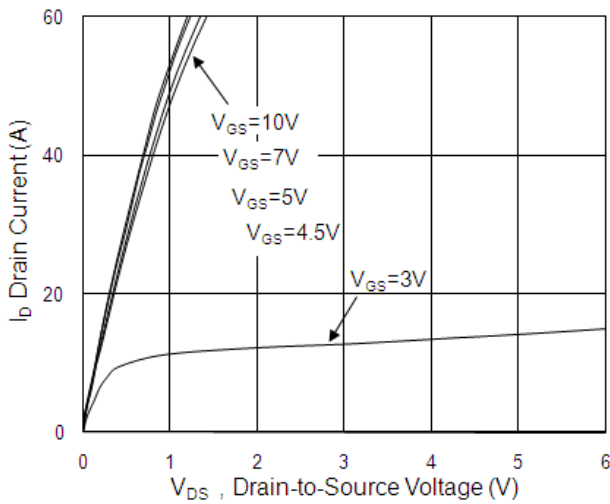


Fig.1 Typical Output Characteristics

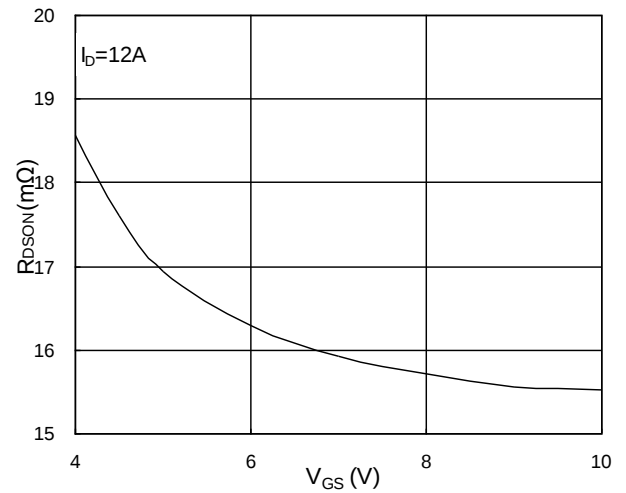


Fig.2 On-Resistance v.s Gate-Source

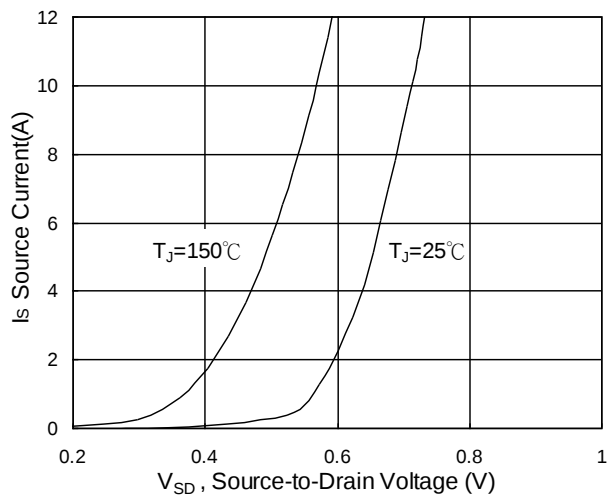


Fig.3 Forward Characteristics of Reverse

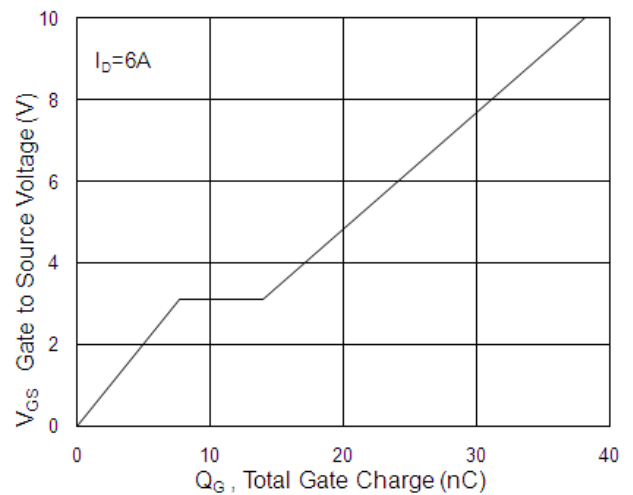


Fig.4 Gate-Charge Characteristics

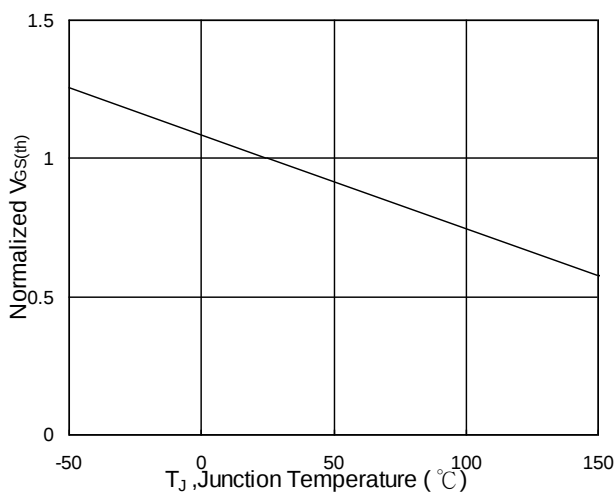


Fig.5 Normalized $V_{GS(th)}$ v.s T_J

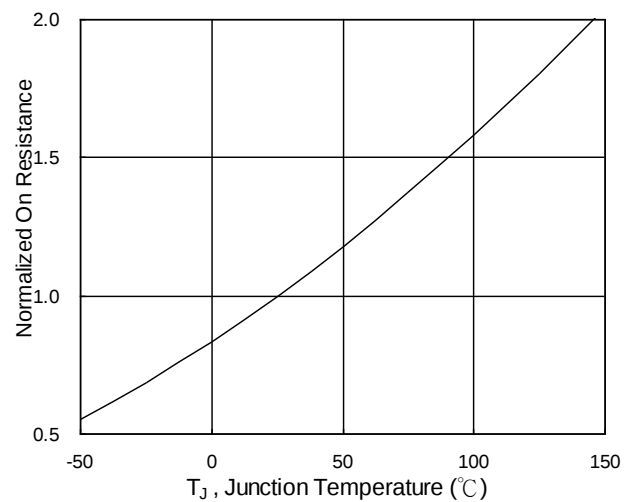
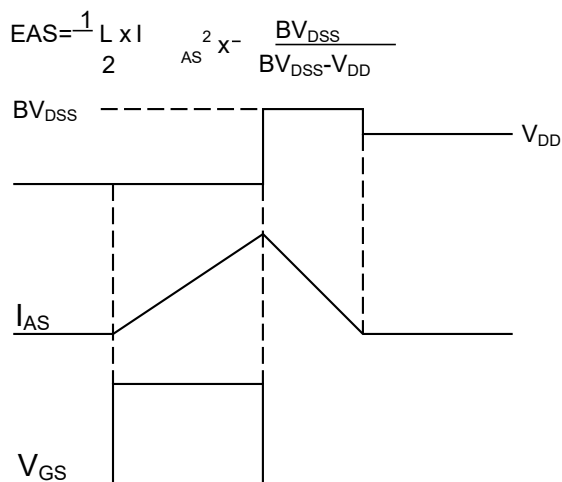
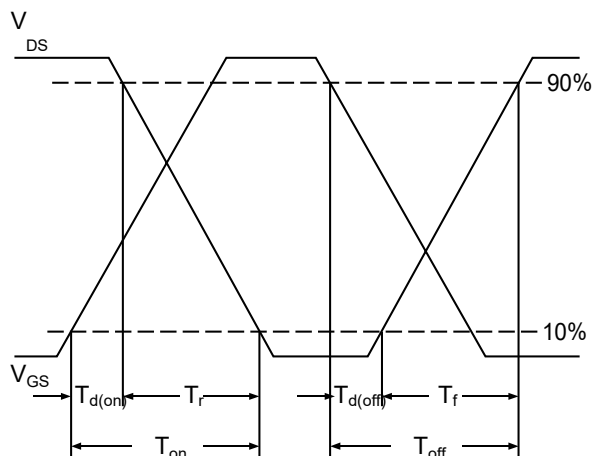
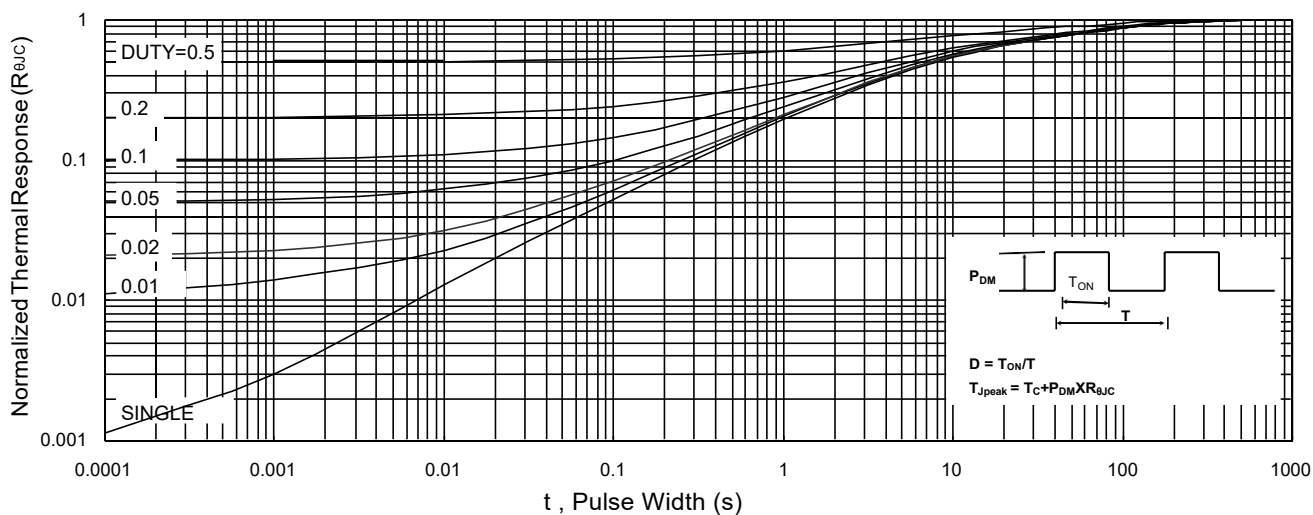
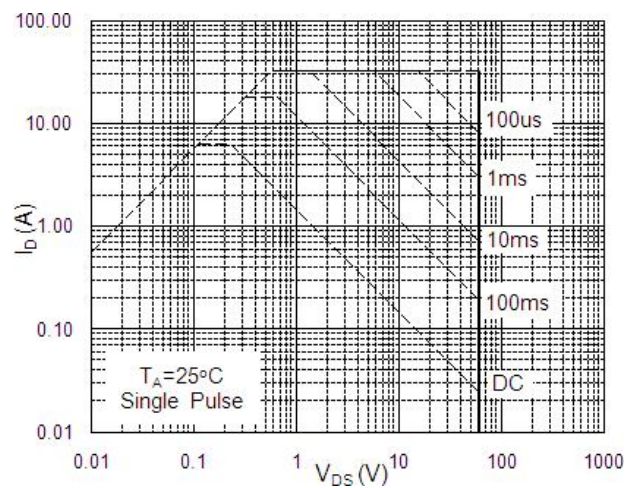
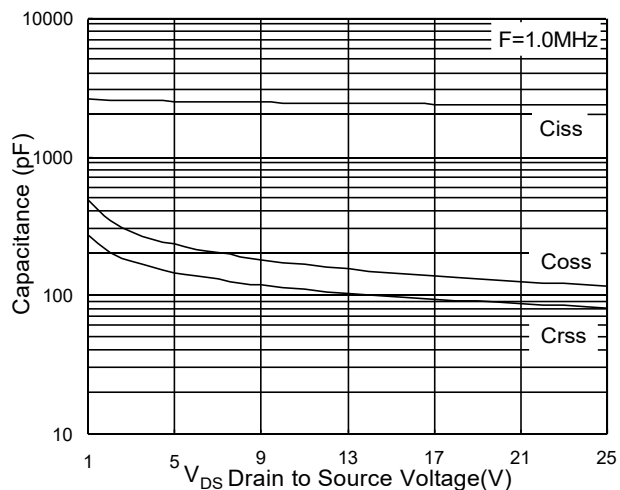
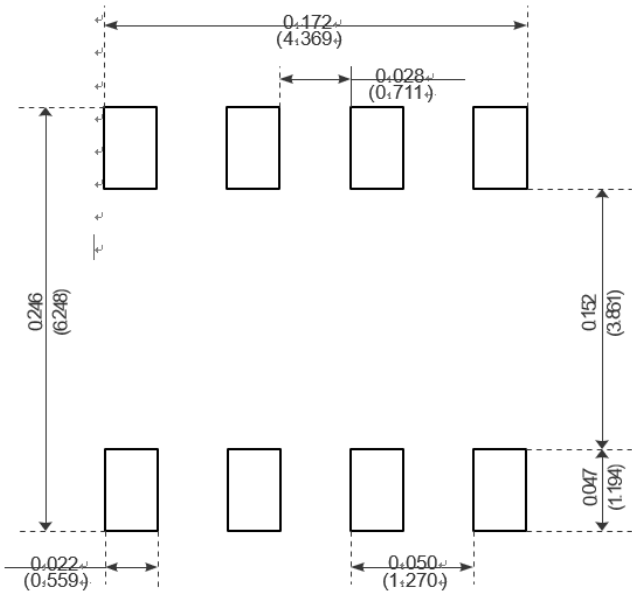
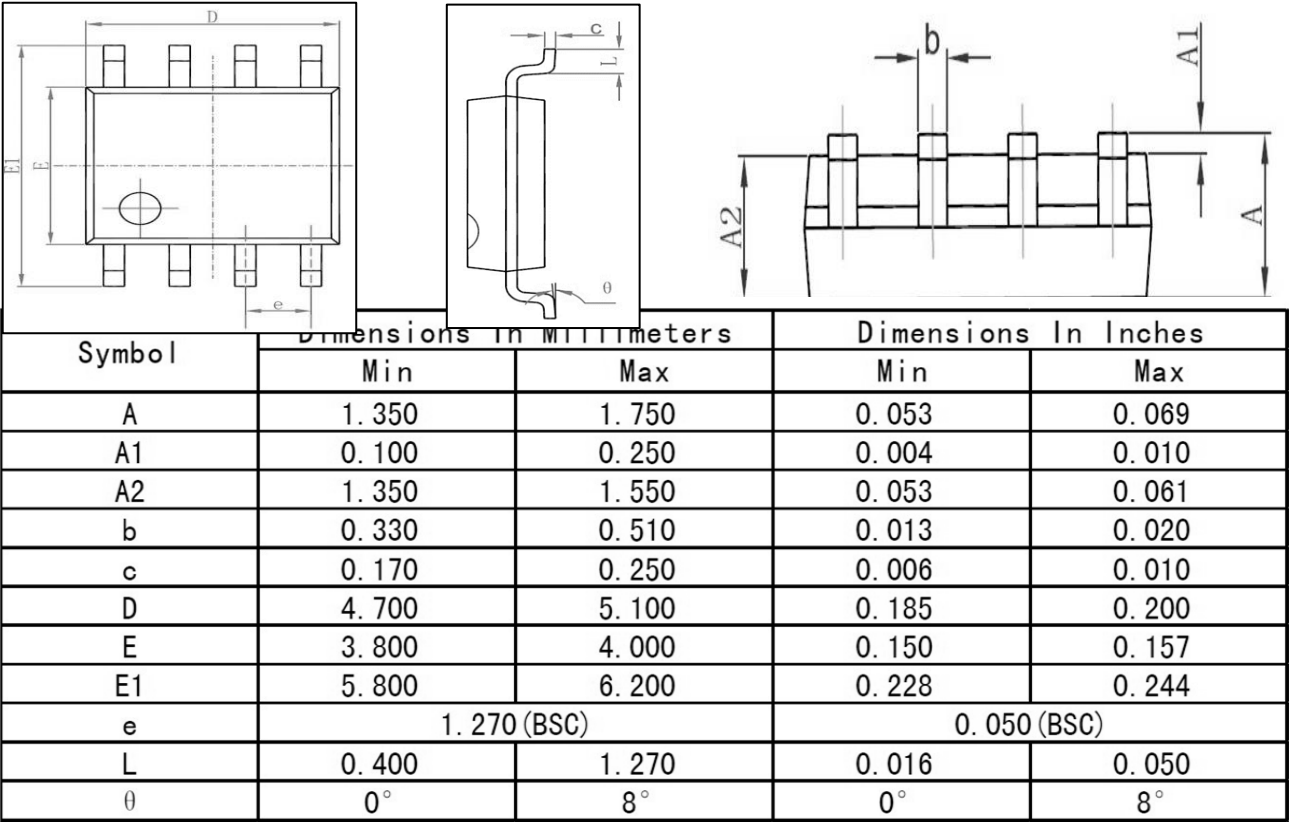


Fig.6 Normalized $R_{DS(on)}$ v.s T_J



Package Mechanical Data-SOP-8



Recommended Minimum Pads